J. Phys. D: Appl. Phys. **42** (2009) 145111 (6pp) doi:10.1088/0022-3727/42/14/145111

Investigation of temperature dependent dc current transport mechanism on Au/poly(4-vinyl phenol)/p-Si device

A Sertap Kavasoglu[1], Cem Tozlu, Osman Pakma, Nese Kavasoglu, Sadan Ozden, Bengul Metin, Ozcan Birgi and Sener Oktik

Faculty of Arts and Sciences, Physics Department, Mugla University, 48170 Mugla, Turkey

E-mail: sertapster@gmail.com

Received 13 February 2009, in final form 21 May 2009
Published 29 June 2009
Online at stacks.iop.org/JPhysD/42/145111

Abstract

In this study, temperature dependent current–voltage (I–V) measurements and investigation of the dc current transport mechanism of Au/poly(4-vinyl phenol)/p-Si device have been performed. While the series resistance value displayed nearly temperature independent behaviour, the ideality factor varied between 7.26 and 2.76 in the temperature range 100–300 K. There is a linear relationship between the barrier height and the ideality factor which is attributed to barrier height inhomogeneities in the Au/poly(4-vinyl phenol)/p-Si device. The temperature dependent ideality factor behaviour shows that thermionic field emission theory is valid rather than thermionic emission theory and the characteristic tunnelling energy is calculated as 65 meV. It is concluded that poly(4-vinyl phenol) is a preferable organic insulator layer with low interface state density because the temperature dependent interface state density calculations give values of the order of $10^{12}\,\mathrm{eV^{-1}\,cm^{-2}}$.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Recently, there has been considerable research on experimental studies of the metal–semiconductor (MS) and metal–insulator–semiconductor (MIS) type Schottky barrier diodes (SBDs) [1–4]. The importance of such studies on MIS type SBDs with native or deposited insulator layers is due to a better understanding of the influence of gate dielectrics on device operation [5]. It is demanded that a dielectric should be a perfect insulator and as thin as possible in order to decrease the operating bias voltages. It is well known that an insulator layer can strongly influence the device characteristics such as the interface state density, Schottky barrier height (SBH) as well as the ideality factor. The performance and stability of these devices are especially dependent on the formation of an insulator layer [6–8]. On the other hand, it has been reported several times that the interface between the insulator and the semiconductor is crucial [9].

Recently, MIS devices, which include organic material as an insulating layer, have become very famous and popular to provide low operating voltage for low power nanoscale devices due to the easy fabrication process as a very thin layer. In this respect, poly(4-vinyl phenol) is an attractive and good candidate as an insulating layer. A few experimental studies have been performed to display the effect of organic material as an insulating layer in device application [8, 10–12]. However, the temperature (T) dependent I–V characteristics of Au/poly(4-vinyl phenol)/p-Si device structure are still unknown. For this reason, a detailed investigation of the electrical characteristics is required to extract the temperature dependent interface state distribution and barrier height (BH) from the measured non-ideal I–V data in the presence of an organic insulating layer.

In this paper, we have investigated the dark forward-bias I–V characteristics of a Au/poly(4-vinyl phenol)/p-Si device in the temperature range of 100–300 K. The forward-bias I–V–T measurements are used to explain the current transport mechanism, inhomogeneity in the barrier and to estimate the

[1] Author to whom any correspondence should be addressed.

 © 2009 IOP Publishing Ltd Printed in the UK

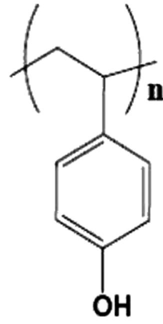

Figure 1. Chemical structure of poly(4-vinyl phenol).

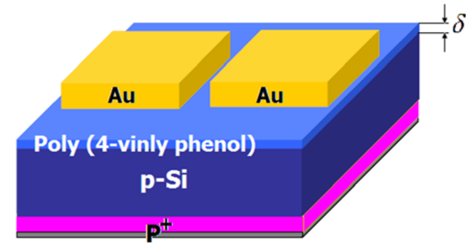

Figure 2. Schematic diagram of the Au/poly(4-vinyl phenol)/p-Si structure.

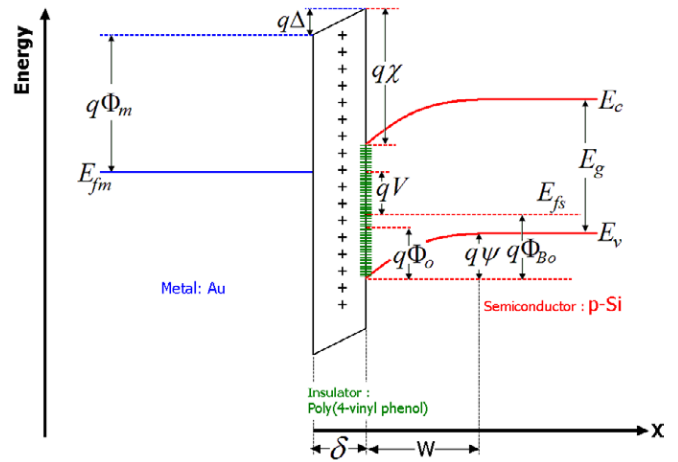

Figure 3. Energy-band diagrams of the Au/poly(4-vinyl phenol)/ p-Si structure.

device parameters. Also, the temperature dependent SBH of Au/poly(4-vinyl phenol)/p-Si device is interpreted based on the existence of lateral inhomogeneities of the BH prevailing at the metal/semiconductor interface.

2. Experimental procedure

A lot of Au/poly(4-vinyl phenol)/p-Si structures were fabricated on a 2 inch diameter float zone ⟨1 1 1⟩ p-type (boron-doped) single crystal silicon wafer with a thickness of 600 μm and a resistivity of 5–10 Ω cm. For the fabrication process, the Si wafer was degreased through the RCA cleaning procedure. The fabrication process of Au/poly(4-vinyl phenol)/p-Si has three major steps used sequentially. (I) Piranha etching (this removes most organic matter): removal of insoluble organic contaminants with 10 min boiling in $NH_4OH + H_2O_2 + 6H_2O$ solution. (II) Oxide strip (RCA process): removal of a thin silicon dioxide layer ($SiO_2 \approx 10$ Å) where metallic contaminants may accumulate as a result of (I), the oxide on the front surface of the substrate was removed in $HF : H_2O(1 : 10)$ solution and finally the wafer was rinsed in de-ionized water for 30 s. (III) Ionic clean: 10 min boiling in $HCl + H_2O_2 + 6H_2O$ solution [13]. Next, it was subjected to a drying process in N_2 atmosphere for a prolonged time. Following the drying process, high-purity aluminium (99.999%) with a thickness of 1500 Å was thermally evaporated from the tungsten filament onto the whole back surface of the Si wafer under a pressure of 10^{-6} Torr. In order to obtain a low-resistivity ohmic back contact, Si wafer was sintered at 580 °C for 3 min in N_2 atmosphere.

The poly(4-vinyl phenol) was purchased from the Sigma-Aldrich firm (Sigma-Aldrich Cat. No 436216) with a molecular weight of 20 000. The chemical structure has been given in figure 1. Spin coating process was applied to cover poly(4-vinyl phenol) on the front surface of the Si wafer from 2.5% solution in 2-proponal at 4000 rpm in 45 s. The obtained film was cross-linked at 100 °C under vacuum. The thickness of the film layer was calculated to be about 141 Å from the high frequency (1 MHz) C–V characteristics. The schematic diagram of Au/poly(4-vinyl phenol)/p-Si structure is given in figure 2.

The measurement was performed inside an evacuated Oxford cryostat. The device was connected to a Keithley 236 Source/Measure unit for dc measurement via a suitably equipped coaxial cable. The measurement was automated with a personal computer. A delay of a few seconds between the subsequent measuring steps was built into the program to assure steady-state conditions for the measurement of the current. In addition, for each voltage step an average of up to 32 current measurements was taken to increase the signal-to-noise ratio and extend the range of current measurement down to 2×10^{-14} A.

3. Results and discussion

The suggested energy-band diagram of the Au/poly(4-vinyl phenol)/p-Si structure under forward bias is shown in figure 3, where Φ_m is the work function of metal, Φ_e is the effective BH, χ is the electronic affinity of the semiconductor, Δ is the voltage drop across the interface insulator layer and δ is the thickness of the insulator layer. The parameter Φ_0 is commonly known as the neutral level of the surface states taken from the valence band edge at the semiconductor surface.

For a SBD in the presence of an insulator layer and other effects, the current depends on the bias voltage. Thermionic emission (TE) theory predicts that the current–voltage characteristic is given as follows [14–24]:

$$I = I_o e^{\frac{q(V-IR_s)}{nk_BT}}\left[1 - e^{-\frac{q(V-IR_s)}{k_BT}}\right], \qquad (1)$$

where I is the measured current, V the applied voltage, R_s the series resistance, q the electronic charge, k_B the Boltzmann constant, T the absolute temperature in kelvin, n the ideality factor that describes departure from the ideal diode equation for

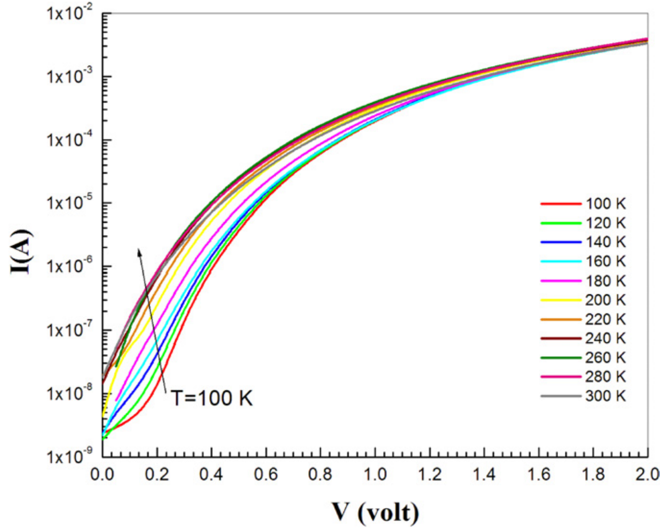

Figure 4. The experimental forward-bias I–V characteristics of the Au/poly(4-vinyl phenol)/p-Si device as a function of temperature.

reverse bias as well as forward bias. I_o is the reverse saturation current derived from the straight-line intercept of ln$I$ at zero bias and is given by

$$I_o = AA^*T^2 e^{-\frac{q\Phi_{Bo}}{k_B T}}, \quad (2)$$

where A is the device contact area, A^* the effective Richardson constant, equal to $32\,A\,cm^{-2}\,K^{-2}$ for p-type Si, and Φ_{Bo} the BH at zero bias, which can be calculated from equation (3):

$$\Phi_{Bo} = \frac{k_B T}{q} \ln\left(\frac{AA^*T^2}{I_o}\right). \quad (3)$$

The ideality factor, n, was extracted using the I–V curves reported in figure 4, according to TE theory. Using equation (1), the value of n is calculated as

$$n = \frac{q}{k_B T}\left[\frac{dV}{d(\ln I)} - IR_s\right]. \quad (4)$$

Under moderately forward-bias condition $((kT/q) > V > 0.4\,V)$, voltage across the series resistance (IR_s) can be neglected. Then, equation (4) is simplified to equation (5):

$$n = \left(\frac{q}{k_B T}\right)\frac{dV}{d(\ln I)}. \quad (5)$$

Using equation (5), the value of n is extracted from the slope of the linear region of the forward-bias ln(I)–V plot.

Measured I–V characteristics of the investigated device structure at various temperatures ranging from 100 to 300 K are given in figure 4. As can be seen in this figure, I–V curves are linear on a semi-logarithmic scale at the moderately forward-bias voltage region, but they depart significantly from linearity at high forward-bias voltages due to the effects of some factors such as series resistance, interfacial insulator layer and interface states.

The series resistance is significant at the high injection region $(2 \geqslant V \geqslant 1.4)$ of the forward-bias I–V characteristics. R_s was extracted using a method developed by Cheung and Cheung [25] in the high-current range where the I–V characteristics is not linear. According to this method, the following function can be rewritten from equation (4):

$$\frac{dV}{d(\ln I)} = IR_s + n\left(\frac{k_B T}{q}\right). \quad (6)$$

Equation (6) should give a straight line for the data of downward-curvature region in the forward-bias I–V characteristic. Thus, a plot of $dV/d(\ln I)$ versus I (figure 5) will give R_s as the slope. The figure inserted in figure 5 shows that the obtained R_s values do not depend on temperature.

Figure 6 shows a plot of the experimental BH versus ideality factor values for various temperatures. The straight line in figure 6 represents the least-squares fit to the experimental data. As can be seen from figure 6, there is a linear relationship between the experimental zero-bias BH and the ideality factors of the investigated device. This result

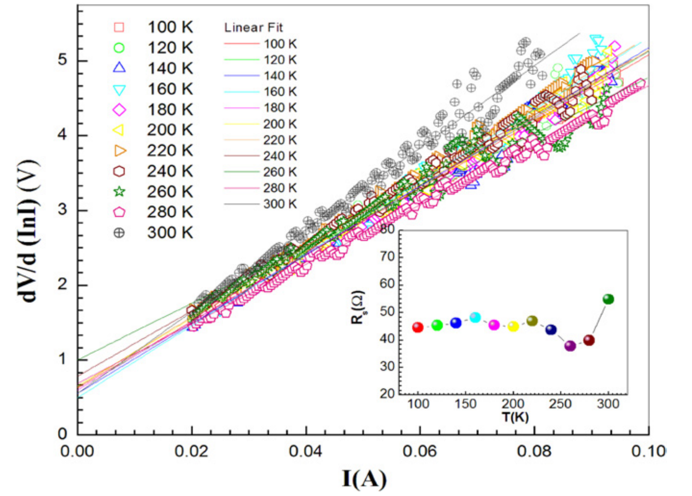

Figure 5. Plots of $dV/d(\ln I)$ versus I of the Au/poly(4-vinyl phenol)/p-Si device.

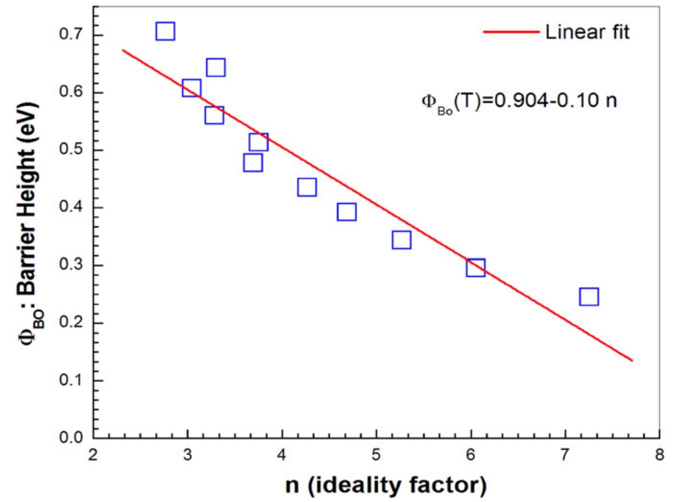

Figure 6. Linear variation of BH versus ideality factors at various temperatures.

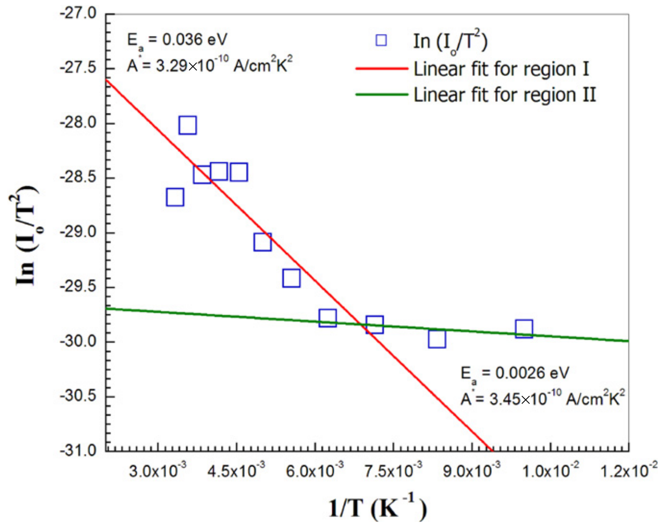

Figure 7. Regular Richardson plot of the saturation current.

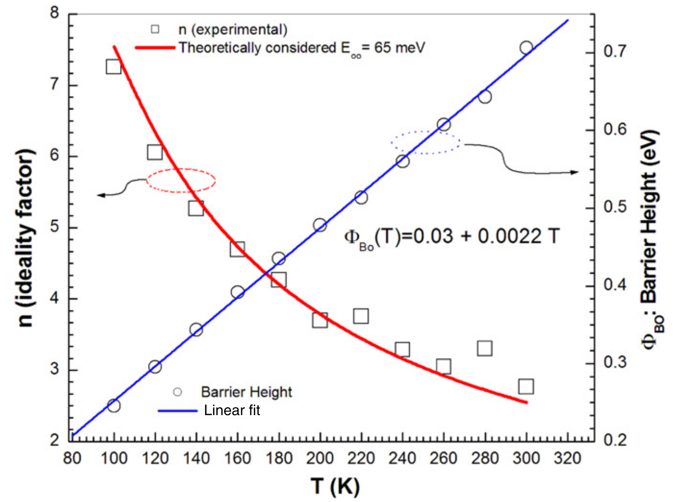

Figure 8. Temperature dependence of zero-bias BH and ideality factor versus temperature for the Au/poly(4-vinyl phenol)/p-Si structure.

can be attributed to lateral inhomogeneities of the BH in the investigated device [14, 26–28].

Interface states in equilibrium with the semiconductor in the Au/poly(4-vinyl phenol)/p-Si device lead to the ideality factor value being significantly greater than unity. Higher values of ideality factors are ascribed to interface dipoles due to interface doping or specific interface structure as well as fabrication-induced defects at the interface. Recently, the barrier modification and ideality properties of the MS contacts with a thin interfacial layer have been studied experimentally [1–12].

As seen in figure 6, variation of Φ_{Bo} with ideality factor changes according to the relation $\Phi_{Bo}(n) = 0.904 - 0.10n$. Using this relation, homogeneous BH value is calculated as 0.804 eV for $n = 1$. Thus, it can be concluded that the significant decrease in Φ_{Bo} and increase in n especially at low temperatures are possibly caused by the BH inhomogeneities.

The Richardson plot of the device is illustrated in figure 7 by means of curve fitting using equation (2). As seen in figure 7, there are two significant linear regions, region I and region II. It is seen that the linear regions of the curve are well fitted with equation (2). At low (100–140 K) and high (160–300 K) temperature regions, the Richardson constant (A^*) has been obtained as 3.45×10^{-10} A cm^{-2} K^{-2} and 3.29×10^{-10} A cm^{-2} K^{-2}, respectively. These values are much lower than the known value of 32 A cm^{-2} K^{-2} for the p-type Si. Such lower values of the Richardson constant obtained from the Richardson plot may be affected by the lateral inhomogeneity of the barrier [29]. The observed behaviour in the Richardson plot may be due to spatially inhomogeneous BH and potential fluctuation at the interface that consists of low and high barrier regions [29]. For this reason, the current through the diode will flow specially via the low barrier in the potential distribution. At low and high temperature regions, activation energy values have been calculated as 0.0026 eV and 0.036 eV, respectively, from the slope of this straight line.

Detailed analysis of barrier inhomogeneities is not within the scope of this work. We have performed barrier inhomogeneities analysis to unveil the inhomogeneities phenomena, which will be presented in a further study.

In order to provide evidence for the presence of BH inhomogeneities, the temperature dependence of the ideality factor can be reported in the form of a plot of n versus T [1–12]. The high values of the ideality factor show that there is a deviation from the TE theory for the current mechanism. The increase in the ideality factor with decreasing temperature is known as the tunnelling effect [19, 22, 28–30]. If the current transport is controlled by the tunnelling field effect (TFE) theory due to the local enhancement of electric field, which can also yield a local reduction of the BH, the relationship between the ideality factor and temperature can be expressed by [22, 28]

$$n = \frac{E_{oo}}{kT} \coth\left(\frac{E_{oo}}{kT}\right), \tag{7}$$

where E_{oo} is characteristic tunnelling energy independent of temperature. The solid curve in figure 8 was plotted by fitting equation (7) to the experimental temperature dependent values of the ideality factor. The open squares in figure 8 show the temperature dependent values of the ideality factor extracted from the experimental current–voltage characteristics in figure 4.

The value of E_{oo} for the Au/poly(4-vinyl phenol)/p-Si device has been found to be 65 meV in the temperature range of 100–300 K from the functional fit to the experimental data (figure 8).

Figure 8 also shows temperature dependent zero-bias BH behaviour. As can be seen in figure 8, the BH increases with increasing temperature. As stated already by Song *et al* [18] and also by Werner and Guttler [19], the increase in the BH with an increase in temperature can be explained by the lateral inhomogeneities of the BH.

The density distribution curves of the interface states in equilibrium with the semiconductor can be determined from the forward-bias I–V characteristics at each temperature. For the investigated device the ideality factor n can be extracted

using equation (8) as

$$n(V) = \frac{q}{k_B T} \frac{(V - IR_s)}{\ln(I/I_0)}. \qquad (8)$$

The effective BH Φ_e is assumed to be bias-dependent due to the presence of an interfacial insulator layer and the interface states located between interfacial insulator layer and semiconductor, and is given by [1–12, 14, 24]

$$\Phi_e = \Phi_{Bo} + \beta(V - IR_s). \qquad (9)$$

Here β is given by $\beta = 1 - [1/n(V)]$.

In a p-type semiconductor, the energy of interface states (E_{ss}) with respect to the top of the valence band E_v at the surface of the semiconductor is given by

$$E_{ss} - E_v = -q\left[\Phi_e - (V - IR_S)\right]. \qquad (10)$$

For the investigated device structure having interface states in equilibrium with the semiconductor, the ideality factor n becomes greater than unity and can be written as

$$n(V) = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_d} + qN_{ss}(V)\right], \qquad (11)$$

where N_{ss} is the density of the interface states in equilibrium with the semiconductor. Equation (11) for N_{ss} as deduced by Card and Rhoderick [15] is reduced to

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_s}{W_d}\right], \qquad (12)$$

where ε_s and ε_i are the permittivities of the semiconductor and the interfacial insulator layer, respectively, δ is the thickness of the insulator layer, W_d is the width of the depletion region. For each temperature, the values of N_{ss} were calculated from equation (12) by substituting $\delta = 141$ Å, $\varepsilon_i = 3.8\varepsilon_o$ and $\varepsilon_s = 11.8\varepsilon_o$. The thickness of the film (organic insulator layer) was calculated from the capacitance measurements (1 MHz) and was found to be about 141 Å, and this can usually make the values of the ideality factor greater than unity [15, 24].

It is seen in figure 9 that the values of interface state density for each temperature are adequately low of the order of 10^{12} eV^{-1} cm^{-2}. From figure 9, for all temperatures an exponential increase in the interface state density is seen from midgap towards the top of the valence band. In addition, some spike-shaped peaks appear as superimposed on these exponential curves. These characteristic peaks together with exponential trends systematically shift towards higher energy with increasing temperature. All N_{ss} values are of the order of 10^{12} eV^{-1} cm^{-2}. It is seen that the observed interface states density for each temperature is quite low compared with similar studies in the literature [1–12]. It is well known that there is an increasing demand for low interface state density MIS-type devices. Thus, one can conclude that poly(4-vinyl phenol) is a usable insulator material for the fabrication of MIS-type devices.

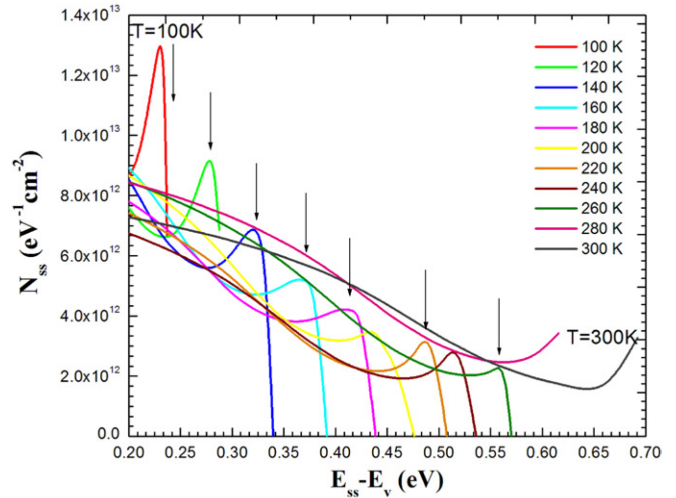

Figure 9. Density of interface states N_{ss} as a function of $E_{ss} - E_v$ deduced from the I–V data at various temperatures for the studied Au/poly(4-vinyl phenol)/p-Si device.

4. Conclusion

The forward-bias I–V characteristics of the Au/poly(4-vinyl phenol)/p-Si device were measured in the temperature range of 100–300 K. The evaluations of the experimental forward-bias I–V characteristics reveal an increase in Φ_{Bo} and a decrease in the ideality factor with increasing temperature. In the studied temperature range, the experimental values of the ideality factor are in agreement with the theoretical curve, which is obtained using the characteristic tunnelling energy value of 65 meV in figure 8. We have claimed that the domination of TFE can be associated with BH inhomogeneities because the enhancement of the transmission probability can be due to the local enhancement of electric field, which can also yield a local reduction of the BH.

The temperature dependence of energy distribution of N_{ss} profiles were extracted from the forward-bias I–V measurements by taking into account the bias dependence of the effective BH Φ_e and the ideality factor n. At the same time, extracted N_{ss} values decrease with increasing values of $E_{ss} - E_v$, for all temperatures. We have also observed characteristic spike-shaped behaviour in our N_{ss} value. A characteristic spike-shaped peak appeared for each maximum and is shifted towards the valence band in the N_{ss} plots with increasing temperature.

References

[1] Tataroglu A and Altındal S 2009 *J. Alloys Compounds* **479** 893–7

[2] Karatas S, Türüt A and Altındal S 2009 *Radiat. Phys. Chem.* **78** 130

[3] Altındal S, Parlaktürk F, Tataroglu A, Parlak M, Sarmasov S N and Agasiev A A 2008 *Vacuum* **82** 1250

[4] Altındal S, Kanbur H, Yıldız D E and Parlak M 2007 *Appl. Surf. Sci.* **253** 5056

[5] Dokme I, Altındal S and Gokcen M 2008 *Microelectron. Eng.* **85** 1910

[6] Yakuphanoglu F, Kandaz M and Senkal B F 2008 *Thin Solid Films* **516** 8793

[7] Yakuphanoglu F 2008 *Sensors Actuators A: Phys.* **147** 104
[8] Yakuphanoglu F 2008 *J. Phys. Chem. Solids* **69** 949
[9] Nicollian E H and Brews J R 1982 *Metal-Oxide Semiconductor (MOS) Physics and Technology* (New York: Wiley)
[10] Gullu O, Aydogan S and Turut A 2008 *Semicond. Sci. Technol.* **23** 075005
[11] Okur S and Yakuphanoglu F 2009 *Sensors Actuators A: Phys.* **149** 241
[12] Yildirim F A, Schliewe R R, Bauhofer W, Meixner R M, Goebel H and Krautschneider W 2008 *Org. Electron.* **9** 70
[13] Kern W 1993 *Handbook of Semiconductor Cleaning Technology* (New York: Noyes)
[14] Rhoderick E H and Williams R H 1988 *Metal–Semiconductor Contacts* 2nd edn (Oxford: Clarendon)
[15] Card H C and Rhoderick E H 1971 *J. Phys. D: Appl. Phys.* **4** 1589
[16] McCafferty P G, Sellai A, Dawson P and Elabd H 1996 *Solid-State Electron.* **39** 583
[17] Chand S and Kumar J 1996 *J. Appl. Phys.* **80** 288
[18] Song Y P, Van Meirhaeghe R L, Laflere W F and Cardon F 1986 *Solid-State Electron.* **29** 33
[19] Werner J H and Guttler H H 1991 *J. Appl. Phys.* **69** 1522
[20] Chand S 2002 *Semicond. Sci. Technol.* **17** L36
[21] Osvald J 2006 *Solid-State Electron.* **50** 228
[22] Horvath Zs J, Dozsa L, Krafcsik O H, Mohacsy T and Vida Gy 2004 *Appl. Surf. Sci.* **234** 67
[23] Singh A 1985 *Solid-State Electron.* **28** 223
[24] Sze S M and Kwog K Ng 2007 *Physics of Semiconductor Devices* 3nd edn (New Jersey: Wiley)
[25] Cheung S K and Cheung N W 1986 *Appl. Phys. Lett.* **49** 85
[26] Gumus A, Turut A and Yalcin N 2002 *J. Appl. Phys.* **91** 245
[27] Iucolano F, Roccaforte F, Giannazzo F and Raineri V 2007 *J. Appl. Phys.* **102** 113701
[28] Aydin M E, Yıldırım N and Turut A 2007 *J. Appl. Phys.* **102** 043701
[29] Tung R T 1992 *Phys. Rev.* B **45** 13509
[30] Padovani F A and Stratton R 1966 *Solid-State Electron.* **9** 695