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ORIGINAL PAPER

The effects of preparation temperature on the main electrical parameters of Al/TiO_2/p-Si (MIS) structures by using sol–gel method

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Abstract In this study, the forward bias current–voltage (*I–V*) and capacitance–voltage (*C–V)* characteristics of the Al/TiO_2/p-Si (MIS) structures derived using the sol–gel method have been investigated and compared at various preparation temperatures. Experimental results show that the preparation temperatures strongly affect the electrical characteristics, such as ideality factor (n), zero-bias barrier height (ϕ_{b0}), series resistance (R_s) and interface states (N_{ss}). The MIS structures show non-ideal behavior of *I–V* characteristics with an n varying between 2.17 and 4.61. We have found that the ϕ_{b0} and R_s increase as the n decrease with increasing preparation temperature. The energy distribution profile of N_{ss} of the Al/TiO_2/p-Si (MIS) structures was obtained from the forward bias *I–V* characteristics by taking into account both the bias dependence of the effective barrier height (ϕ_e) and R_s for various preparation temperatures. The values of N_{ss} increase from the midgap towards the top of valance band for various preparation temperatures.

Keywords Sol–gel method · Al/TiO_2/p-Si (MIS) structures · Preparation temperature · Interface state density · Series resistance

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1 Introduction

The various non-idealities, such as the formation of insulator layer at metal/semiconductor interface, the energy distrubution profile of interface states at semiconductor/insulator interface, series resistance and inhomogeneous Schottky barrier heights affect the electrical characteristics of metal–insulator–semiconductor (MIS) structures. The insulating layer in the MIS structures seperates the metal and semiconductor and creates a continuous distribution of surface states at semiconductor/insulator interface [1, 2]. Although a vast number of publications report on the experimental studies on electrical characteristics parameters, such as the ideality factor, barrier height, series resistance and surface states in metal–semiconductor (MS) and MIS structures, a satisfactory understanding of all details has not been achieved yet [3–19].

Used in semiconductor technology, Si is a source amply found in nature; moreover, one another important characteristic of Si is that it allows the formation of an insulator layer on the crystal surface of SiO_2. Recently, the formation of an insulator layer on Si substrate, such as SnO_2, [20] Si_3N_4, [4] and TiO_2 [21] films has been investigated as a potential material to replace silicon-dioxide (SiO_2). The titanium dioxide (TiO_2) thin films have been extensively studied because of their interesting chemical, optical and electrical properties. It has three different crystalline modifications: anatase, rutile and brookite [22]. Among these crystals, anatase TiO_2 has attracted a great deal of interest because of its excellent photocatalytic behavior. It is, however, difficult to synthesize anatase TiO_2 films because this phase is thermodynamically more unstable than the rutile phase [22, 23]. Various techniques used for the preparation of TiO_2 films include sputtering, [24] e-beam evaporation, [25] chemical vapor deposition [26]

and sol–gel process [27, 28]. The sol–gel method is one of the most promising methods since optical and other properties of thin films can be easily controlled by changing the solution composition and deposition condition.

In general, the forward bias *I–V* characteristics at intermediate voltages region show a linear behavior in the semi-logarithmic scale. When the applied voltage is sufficiently high ($V \geq 0.8$ V), the linearity considerably deviates due to series resistance and surface states [2, 3]. On the other hand, the high values of ideality factor of MIS structure can be explained by means of the effects of the bias voltage drop across the insulator layer thickness, surface states, bias dependence of barrier height and barrier inhomogeneity [1, 29].

In this study, the authors examined the effects of preparation temperature on the main electrical parameters of Al/TiO_2/p-Si MIS structures prepared using the sol–gel dip-coating method. The energy distribution profile of interface states for structures at various preparation temperatures was obtained from the forward bias *I–V* characteristics by taking into account the series resistance and bias dependence of effective barrier height of Al/TiO_2/p-Si (MIS) structures at room temperature. Other main electrical parameters such as ideality factor (n), zero-bias barrier height (ϕ_{b0}), doping concentration (N_A) and depletion layer width (W_D) of Al/TiO_2/p-Si MIS structures were also determined at the same conditions.

2 Experimental

In order to prepare a TiO_2 solution, firstly 1.2 mL titanium tetraispropoxide [$Ti(OC_3H_7)_4$, ex. Ti $\geq$ 98%, Merck] was added in 15 mL ethanol [C_2H_6O, 99.9%, Merck] and the solution was kept in a magnetic stirrer for 1 h. Then, 5 mL glacial acetic acide [$C_2H_4O_2$, 99.9%, Merck] and 10 mL ethanol were added in the solution and after each additive component is added, it was mixed in the magnetic stirrer for 1 h. As a final step, 1.5 mL trietilamine [$(C_2H_5)_3N$, 99%, Merck] was added in the solution and the final solution was subjected to the magnetic stirrer for 3 h. The solution was aged at room temperature for 1 days before deposition.

A lot of MIS (Al/TiO_2/p-Si) structures were fabricated on the 5-inch diameter float zone <111> p-type (boron-doped) single crystal silicon wafer with a thickness of 600 μm and a resistivity of 5–10 Ω cm. For the fabrication process, Si wafer was degreased through RCA cleaning procedure. The RCA cleaning procedure has three major steps used sequentially: I. Organic Clean: Removal of insoluble organic contaminants with a 10-min boiling in $NH_4OH + H_2O_2 + 6H_2O$ solution. II. Oxide Strip: Removal of a thin silicon dioxide layer ($SiO_2 \approx 10$ Å) where metallic contaminants may accumulated as a result of (I), using a diluted (30 s) HF:H_2O (1:10) solution. III. Ionic Clean: A followed by a 10-min boiling in $HCl + H_2O_2 + 6H_2O$ solution [30]. Next, it was subjected to the drying process in N_2 atmosphere for a prolonged time. Following the drying process, high-purity aluminum (99.999%) with a thickness of 1,500 Å was thermally evaporated from the tungsten filament onto the whole back surface of the Si wafer under the pressure of 10^{-7} Torr. In order to obtain a low-resistivity ohmic back contact, Si wafer was sintered at 580 °C for 3 min in N_2 atmosphere.

The dipping process was performed using a home-made motorized unit and each sample was dipped into the solution three times. After each cleaned p-type silicon crystal was dipped into the solution, one substrate of alloy formed on the surface of Si wafer was cleaned with ethanol. After each dipping process, samples were subjected to repeated annealing processes at the temperature of 200 °C for 5-min period. Finally, the samples were post-annealed at the temperature of 500 °C for 1 hour in air using an electric oven (Vecstar VCTF-4).

In order to obtain a rectifying contact on the front surface of p-Si coated with TiO_2, a high-purity aluminium layer (99.999%, 2,000 Å) was coated on the surface in a high vacuum under the pressure of 10^{-7} Torr. Metal layer thickness and the deposition rate were monitored using Inficon XTM/2 thickness monitor. The interfacial insulator layer thicknesses were estimated to be about 63, 89 and 102 Å by spectroscopic ellipsometry (VASE M2000, Woolam).

The current–voltage (*I–V*) measurements were performed using a Keithley 2,420 programmable constant current source. The forward and reverse bias capacitance–voltage (*C–V*) measurements were performed by using an HP 4,192 A LF impedance analyzer (5 Hz–13 MHz) at 1 MHz and with a test signal of 50 mV_{rms}. All measurements were carried out at room temperature and in a dark environment.

3 Results and discussion

When a MS structure with a series resistance (R_s) is considered, according to the thermionic emission (TE) current corrected by tunneling, it is assumed that the relation between the applied forward bias voltage V ($V \geq 3kT/q$) and the current I is expressed as [2]

$$I = I_o \exp\left(\frac{q(V - IR_S)}{nkT}\right)\left[1 - \exp\left(\frac{-q(V - IR_S)}{kT}\right)\right], \quad (1a)$$

where I_0 is the reverse saturation current derived from the straight line intercept of the current zero bias and is given by

$$I_0 = AA^*T^2 \exp\left(-\frac{q\phi_{b0}}{kT}\right), \quad (1b)$$

where ϕ_{b0}, IR_s, A, A^*, n, q and T are zero-bias barrier height, voltage drop across series resistance of structure, the rectifier contact area (=4 × 10^{-3} cm^2), the effective Richardson constant (32 A/cm^2K^2 for p-type Si), the ideality factory, the electron charge and the temperature in Kelvin, respectively. For an MS structure with an interfacial insulator layer native or deposited, the expression for the saturation current should written as

$$I_0 = AA^*T^2 \exp(-\alpha\chi^{0.5}\delta) \exp\left(-\frac{q\phi_{b0}}{kT}\right), \quad (2)$$

where $\alpha = (4\pi/h)(2m^*)^{1/2} = 0.526eV^{-1/2}$ Å^{-1} is a constant that depends on the tunneling effective mass ($m^* = 1.51 \times 10^{-12}$ eV s^2 m^{-2}) and Planck's constant ($h = 4{,}135 \times 10^{-15}$ eV s), c, is the effective tunneling barrier of the TiO_2 layer to holes and d is the thickness of the interfacial layer in which holes move through tunnel, respectively.

The values of ideality factor are obtained from the slope of the linear region of the forward bias *lnI–V* plots for various prepared temperatures, and can be obtained as from Eq. 1a

$$n = \frac{q}{kT}\frac{d(V - IR_S)}{d(\ln I)}, \quad (3)$$

Also, the voltage-dependent ideality factor $n(V)$ can be obtained as from Eq. 1a

$$n(V) = \frac{q}{kT}\frac{(V - IR_S)}{\ln(I/I_0)}, \quad (4)$$

Figure 1 shows the experimental forward and reverse bias *lnI-V* characteristics of Al/TiO_2/p-Si (MIS) structures prepared at various preparation temperatures as 100, 200 and 300 °C, at room temperature. As can been seen in Fig. 1, the *lnI-V* characteristics of Al/TiO_2/p-Si (MIS) structures show rectifying behavior. The rectification ratios have the factors of 159 (at 100 °C), 400 (at 200 °C) and 5,223 (at 300 °C) achieved between the reverse and forward bias current at ±2 V where the reverse bias current saturates.

As it is known, the characteristic *lnI-V* graph of a diode usually has three regions, which are low voltage region ($V \leq 0.1$ V), medium voltage region (0.1 V $\leq V \leq$ 0.8 V), and high voltage region ($V \geq 0.8$ V), respectively. The electrical parameters except for R_s were calculated in the linear region in the medium voltage region, while R_s was calculated in the region where the *lnI-V* curve in the high voltage region bended. As can be seen Fig. 1, the each semilogarithmic *I–V* curve consists of a linear range with different slopes in between the intermediate-bias voltage ($0.07V \leq V \leq 0.45V$) regions. The determined values of the

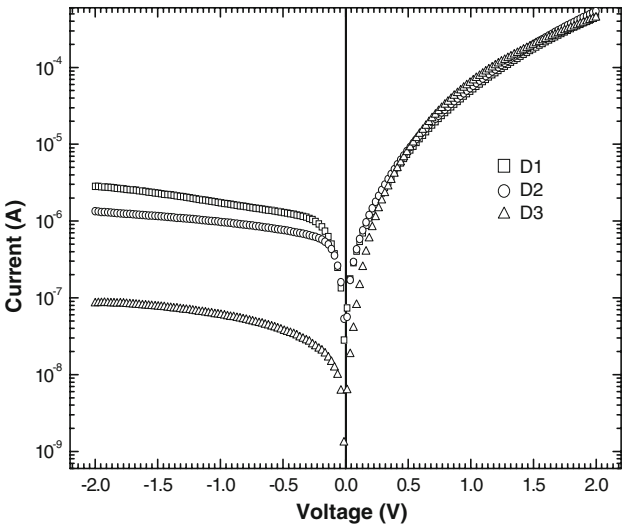

Fig. 1 Forward and reverse bias *I–V* characteristics of Al/TiO_2/p-Si (MIS) structures at room temperature

ideality factor (n) range from 2.17 (at 300 °C) to 4.61 (at 100 °C). It is obvious that the ideality factors of the structures are considerably larger than unity. These values of n show that the device obey a MIS configuration rather than MS contacts. Therefore, these high values of ideality factor especially can be attributed to the presence of an insulator layer and a wide distribution of low Schottky barrier height (SBH) patches at at M/S interface, and particular distribution of interface states at Si/TiO_2 interface [3–6].

The values of saturation current I_0 of samples were obtained by extrapolating the linear intermediate bias voltage region to zero bias for each preparation temperature. The calculated values I_0 and n are given in Table 1. These experimental results show that n decreases with increasing preparation temperature.

As shown in Fig. 1, the series resistance (R_s) is an important parameter, particularly in the downward curvature of the forward bias *I–V* characteristics at a sufficiently high bias voltage. As the linear range of the forward bias *I–V* plots are reduced, the accuracy of the determination of ϕ_{b0}, n and surface states (N_{ss}) becomes unreliable. Therefore, the values ofϕ_{b0}, n and R_s were obtained using a method developed by Cheung and Cheung. The Cheung's functions are given as

$$\frac{dV}{d(\ln I)} = IR_s + n\left(\frac{kT}{q}\right), \quad (5a)$$

$$H(I) = V - n\frac{kT}{q}\ln\left(\frac{I}{AA^*T^2}\right) = n\phi_b + IR_s, \quad (5b)$$

Figure 2 shows the experimental $dV/d(lnI)$ vs I, and $H(I)$ vs I plots for the Al/TiO_2/p-Si (MIS) structure for three preparation temperatures, respectively, at room

Table 1 Various parameters obtained from *I* to *V* and *C* to *V* (1 MHz) characteristics of Al/TiO_2/p-Si (MIS) structures at room temperature

Samples	TiO_2 films; repeated annealing temperatures (°C)	δ (Å)	I_0 (A)	n	$\phi_{b0}(I$–$V)$ (eV)	R_S (dV/dLn(I)) (Ω)	R_S (H(I)) (Ω)	$\phi_{b0}(C$–$V)$ (eV)	V_d (eV)	$\alpha\chi^{0.5}\delta$	N_A (cm^{-3})
D1	100	102	7.53×10^{-8}	4.61	0.647	523.21	482.18	0.448	0.372	7.83	8.63×10^{15}
D2	200	89	2.54×10^{-8}	3.42	0.663	617.12	527.53	0.491	0.416	7.20	9.18×10^{15}
D3	300	63	1.48×10^{-9}	2.17	0.710	691.22	627.33	0.700	0.633	1.68	2.01×10^{15}

temperature. As can be seen in Fig. 2a and b, these figures should give a straight line for downward curvature region. Thus, the values of n and R_s were obtained from the intercept and slope of the *dV/d(lnI)* vs *I* plots (Fig. 2a) at each preparation temperature. Using the n value calculated from Eq. 5a, plots of *H(I)* vs *I* will also give a straight line with a current axis intercept equal to $n\phi_b$. The slope of this plot also provides a second determination of R_s, which can be used to check the consistency of this approach. The determined values of series resistance ranged from 523.21 and 482.18 Ω (at 100 °C) to 691.22 and 627.33 Ω (at 300 °C), respectively, and are also given in Table 1.

The R_s is significant in the downward curvature of the forward bias *I*–*V* characteristics, but the interface states (N_{ss}) are effective in all forward bias region and their distribution changes from region to region in the band gap at semiconductor/insulator interface. The energy density distribution profile of these interface states N_{ss} for Al/TiO_2/p-Si (MIS) structures can be obtained from the forward bias *I*–*V* characteristics by taking into account the bias dependence of the ideality factor, barrier height and series resistance. The voltage dependence of the barrier height (ϕ_e) is contained in the ideality factor n through the relation [11] as

$$d\phi_e/dV = \beta = 1 - 1/n, \tag{6}$$

where β is the voltage coefficient of the effective barrier height. The effective barrier height is given by [12, 13].

$$\phi_e = \phi_{b0} + \beta(V - IR_S) = \phi_{b0} + \left(\frac{d\phi_e}{dV}\right)(V - IR_S), \tag{7}$$

where $d\phi_e/dV$ is the change in the barrier height with bias voltage.

For the MIS structure with N_{ss} which is in equilibrium with semiconductor, the expression for the N_{ss} deduced by Card and Rhoderick [2, 3] is reduced as

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_s}{W_D}\right], \tag{8}$$

where δ is the thickness of the interfacial insulator layer (TiO_2), W_D is the depletion layer width, $\varepsilon_s = 11.8\varepsilon_0$,

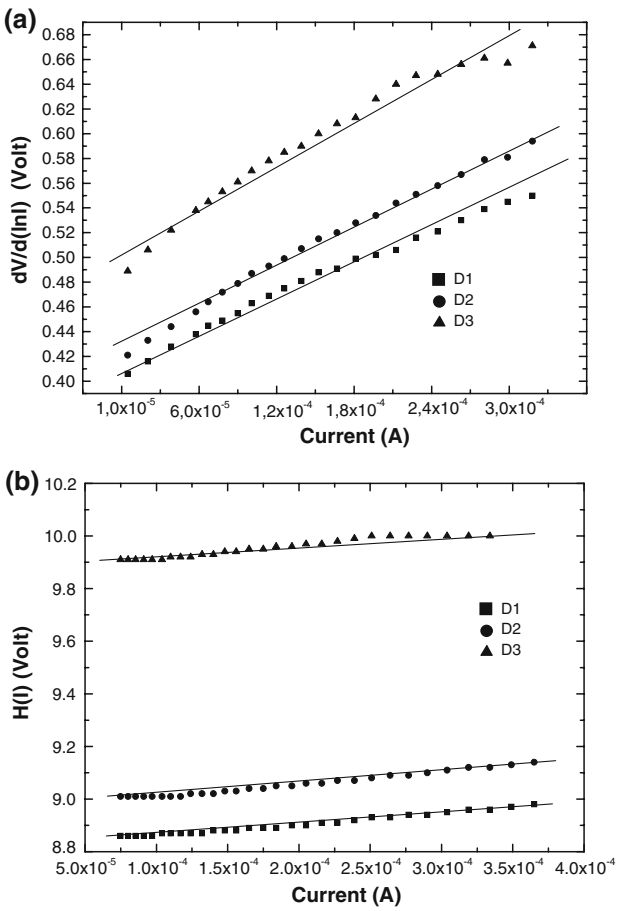

Fig. 2 **a** d*V*/d(*lnI*)- *I* and **b** *H*(*I*)-*I* characteristics of the Al/TiO_2/p-Si (MIS) structures at room temperature

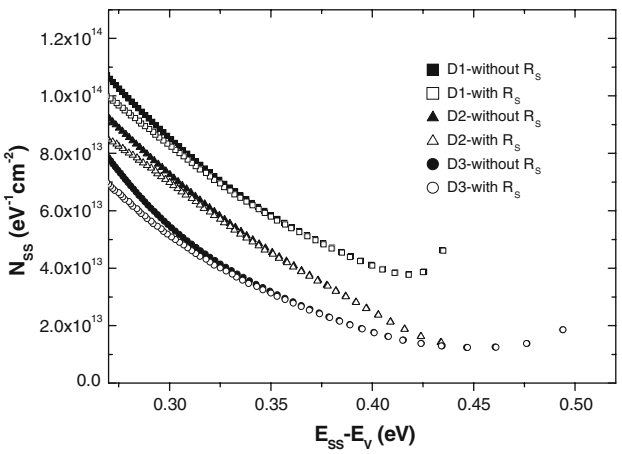

Fig. 3 The energy distribution profile of interface states obtained from the forward bias *I*–*V* characteristics of Al/TiO_2/p-Si (MIS) structures at room temperature

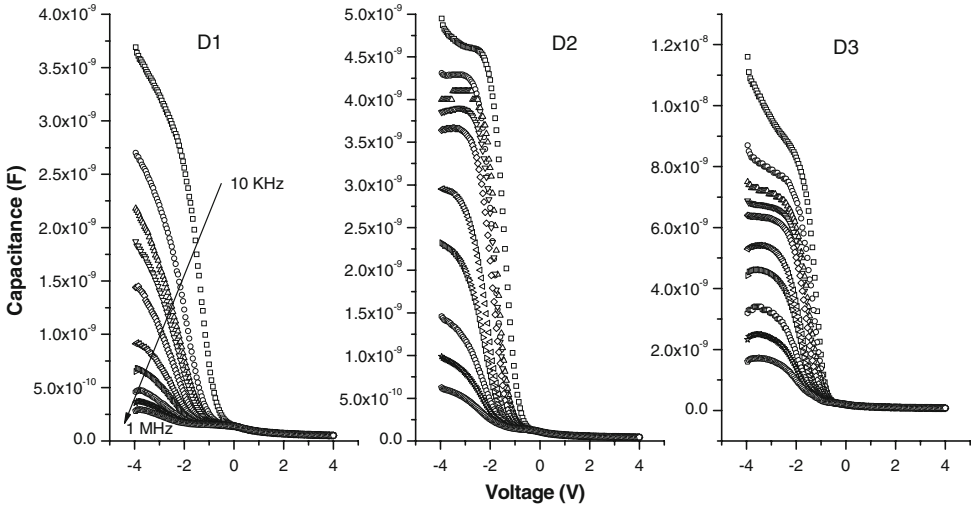

Fig. 4 The *C–V* characteristics of Al/TiO_2/p-Si MIS structures at various frequency at room temperature

$\varepsilon_i = 48\varepsilon_0$ [31, 32] and ε_0 is the permittivity of the free space. For p-type semiconductors, the energy of the interface states E_{ss} with respect to the bottom of the valance band at the surface of semiconductor is given as [3, 11]

$$E_{ss} - E_v = q[\phi_e - (V - IR_S)], \tag{9}$$

The energy distribution profile of the interface states for Al/TiO_2/p-Si (MIS) structure was obtained from Eq. 8 by taking into account R_s values from the experimental forward bias *I–V* characteristics at each preparation temperature and is given in Fig. 3. As can be seen in Fig. 3, the increase in the values of interface states for various preparation temperatures from mid gap towards the top of valance band is very apparent. It is obvious that the values of N_{ss} decrease with increasing preparation temperatures. Such behavior of N_{ss} is a result of molecular restructuring and reordering of the metal–semiconductor–interface (Al/TiO_2/p-Si) under the temperature effect [16]. The magnitude of the N_{ss} with and without the R_s at 0.24-E_v ranged from 3.84×10^{13} and 1.06×10^{14} $eV^{-1}cm^{-2}$ (at 100 °C) to 1.18×10^{13} and 7.75×10^{13} $eV^{-1}cm^{-2}$ (at 300 °C), respectively. Furthermore, experimental results show that the values of N_{ss} obtained by taking into account the R_s are lower than those of without the R_s, particularly near the valance band. Similar results have been reported in literature [16–18].

The capacitance–voltage–frequency (*C–V–f*) characteristics of Al/TiO_2/p-Si (MIS) structures were measured at various frequency (10, 30, 50, 70, 100, 200, 300, 500, 700 KHz and 1 MHz) are given in Fig. 4, respectively. At low frequencies, the N_{ss} can easily follow the ac signal and yield an excess capacitance, which depends on frequency and time constant of interface states [1, 19]. However, in sufficiently high frequency limit ($f \geq 500$ kHz), the N_{ss} can hardly follow the ac signal and the contribution of interface states capacitance to the total capacitance may be neglected. The *C–V* characteristics at 1 MHz for three various preparation temperatures are given in Fig. 5. In order to obtain the doping concentration (N_A), diffusion potential (V_d), depletion layer width (W_D), and barrier height ($\phi_{b0}(C - V)$), C^{-2} vs V plots were obtained from Fig. 5 and are given in Fig. 6. The *C–V* relationship for an ideal MIS structure can be expressed as [1, 19]

$$C^{-2} = \frac{2(V_d + V)}{\varepsilon_s \varepsilon_0 q A^2 N_A}, \tag{10}$$

$$\frac{d(C^{-2})}{dV} = \frac{2}{\varepsilon_s \varepsilon_0 q A^2 N_A}, \tag{11}$$

where V_d and N_A are the diffusion potential and doping concentration of boron atoms. The values of V_d were determined from the extrapolation of the linear part of C^{-2} vs V (Fig. 6) plot to voltage axis, while the values of N_A were calculated from the slope of the same plot at 1 MHz.

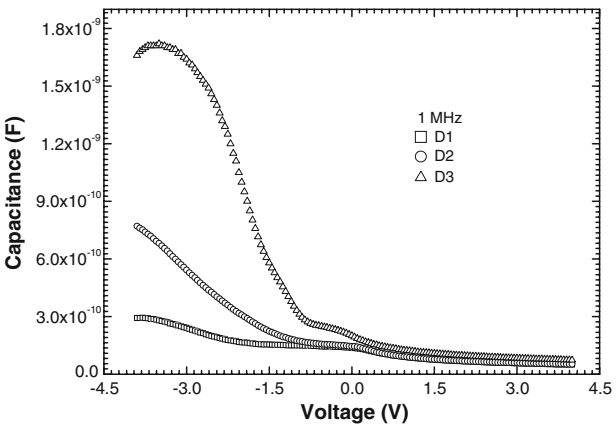

Fig. 5 High frequency (1 MHz) *C–V* characteristics of Al/TiO_2/p-Si (MIS) structures at room temperature

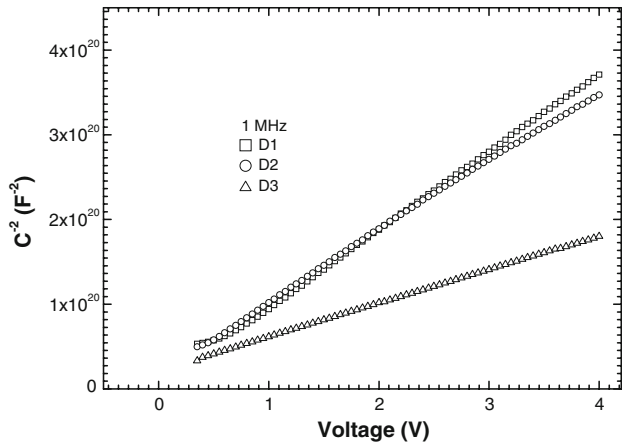

Fig. 6 The C^{-2}–V characteristics of the Al/TiO_2/p-Si (MIS) structures at room temperature

The barrier height obtained from C to V data can be expressed as

$$\phi_{b0} = V_0 + \frac{kT}{q} + E_F, \tag{12}$$

where V_0 is intercept or built-in voltage and E_F is the Fermi energy measured from the valance band edge for p-type Si. The values of V_0 were calculated by extrapolating C^{-2} vs V plots to the voltage axis and the values of barrier height ($\phi_{b0}(C-V)$) were calculated from Eq. 12 for each preparation temperature. These values are given in Table 1 at various preparation temperatures. As can be seen in Table 1, the values of N_A, V_d and $\phi_{b0}(C-V)$increase with increasing preparation temperatures.

4 Conclusions

The forward and reverse bias I–V and C–V characteristics of the Al/TiO_2/p-Si (MIS) structures derived using the sol–gel method were measured at room temperature for structures prepared at various preparation temperatures. Experimental results show that preparation temperatures have a strong effect on the I–V and C–V characteristics. These high values of ideality factor can be attributed to the presence of a wide distribution of low Schottky barrier height (SBH) patches, insulator layer thickness, the particular distribution of N_{ss} at Si/TiO_2 interface, and the R_s of structure. While the values of ϕ_{b0}, R_s and N_A increased with increasing preparation temperature, the n showed a decrease. The determined $\phi_{b0}(I$–$V)$ obtained from I–V and $\phi_{b0}(C-V)$ obtained from C–V increase with increasing preparation temperatures.

The energy distrubution profile of N_{ss} of the Al/TiO_2/p-Si (MIS) structures were obtained from the forward bias current–voltage (I–V) characteristics by taking into account both the bias dependence of the effective barrier height (ϕ_e) and R_s for various preparation temperatures. The values of the N_{ss} with and without the R_s at 0.24-E_v ranged from 3.84×10^{13} to 1.06×10^{14} $eV^{-1}cm^{-2}$ (at 100 °C) and 1.18×10^{13} to 7.75×10^{13} $eV^{-1}cm^{-2}$ (at 300 °C), respectively, which is a result of molecular restructuring and reordering of the MIS (Al/TiO_2/p-Si) under the temperature effect.

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